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An Improved Performance Full Adder

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Abstract- A lot of research has been going on Full Adder in the current years due to some application or some technology. Full Adder is most significant unit in digital signal processing application. Full adder technologies are entering a new phase. The full adder cell proposed exhibit better-quality variability utilizing MTCMOS technique which is an effective technique for circuit-level designing. The proposed full adder cell is simulated using Tanner EDA tool at 45nm technology for different voltages. The proposed Full Adder design offers significant upgradation in terms of power and speed.

Keywords: *MTCMOS technique, full adder, circuit-level design.*

I. Introduction

The low power integrated circuits (ICs) are designed at different design levels, like circuit, architecture, physical design and process technology. CMOS ICs have been changing into low voltage and low power regimes [1], [2]. Today, VLSI industry has been concentrating on high performance microprocessors. Increased demand for high performance arithmetic units in image processing units, floating point processors and digital signal processing has led to the growth of high-speed adders since these devices need low-power, high speed operation[3].

CMOS circuits are the basic building blocks of digital electronics. The continuous scaling of MOS transistors and reduction in chip area makes power consumption of main concern in VLSI design. Power reduction is of main concern as leakage and dissipation causes overheating problem, reduces performance and lifetime of the chip. It can be reduced by scaling the supply voltage and device geometry but it affects the speed of the circuit [4]. So an alternate to design logic gates working at high speed with relatively lesser power dissipation is MTCMOS technique. It reduces the sub-threshold current in standby mode while preserving circuit performance. It is also useful to increase level of integration, feasibility and reliability [8].

the carry can be obtained as the sum of products of all the three bits i.e. $AB+BC+AC$. Basic full adder design is shown in Fig 1. Expressions for Sum 'S' and carry 'COUT' are given by equation (1) and (2) [7].

$$S = A \oplus B \oplus C_{IN}$$

$$C_{OUT} = AB \oplus BC \oplus AC$$

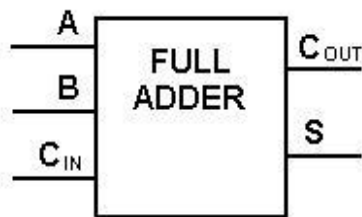


Fig. 1 Basic Full Adder

Table-I Truth table for full adder

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

II. ADDERS

2.1 Full Adder

A full-adder is a circuit which is used to add three bits at a time. It finds application in many digital circuits like calculators, processors, etc. It can also be implemented using two half adder circuits i.e. by feeding two inputs say A and B to one half-adder to get the sum and carry of given bits[5]. The sum output is then fed to other half-adder along with the third input C_{IN} to obtain the sum of all the three bits i.e. A , B and C and their carry output. The carry of both the full adders are then ORed to get the carry 'COUT'.

A full-adder has three input terminals and two output terminals sum and carry. The sum of a full adder can be calculated by Ex-ORing the three bits i.e. $A \oplus B \oplus C$ while

Equation (3) gives the total power dissipation of a CMOS circuit

$$P_{total} = P_d + P_{sc} + P_s$$

Where P_d is the dynamic power, P_{sc} is the short-circuit power and P_s is the static power dissipation.

III. MTCMOS Technique

MTCMOS technique is a technique which can be applied for reducing leakage current in low voltage circuits. In the standby mode is based on using two different type of transistor (n-MOS & p-MOS) with 2 different V_T in the circuit. Low threshold transistor are usually used to design logic gates where switching speed is significant, whereas high V_T transistor are used to effectively separate the logic gates in standby mode & stop leakage dissipation. Transistors in active mode transistor are turned on & logic gate consisting of low V_T transistor can operate with low switching power dissipation & small propagation delay. High-threshold transistors are turned ON in active mode while in standby mode the high-threshold transistor is turned OFF.

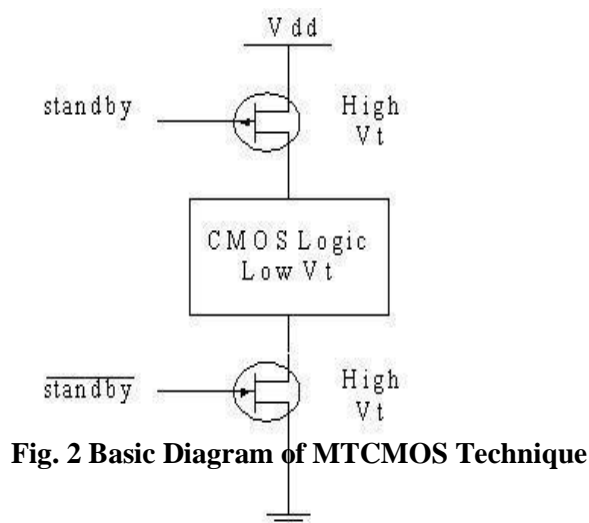


Fig. 2 Basic Diagram of MTCMOS Technique

The MTCMOS technology has 2 main features. For efficient power management *Active* and *Sleep* mode of operations are associated with this technique and transistors operating at high and low threshold voltages (V_T) are used for circuit designing.

IV. Existing Full Adder

The existing circuit shown in Fig.3 can further be explained by 3 blocks. Each block is designed separately for improvement in power and delay. The execution of XNOR module by the sum of full adder output [1].

In this existing circuit some power related problems occur so in proposed circuit we reduce all the problems. Through XNOR circuit we can consume the power but some power is lost at implementation time. Transistor pmos_1 and nmos_1 make Z; the controlled inverter can be designed successfully using it. The output of this controlled inverter is obtained by XNORing the inputs A and B. Pass transistors pmos_3 and nmos_3 are used for eliminating the voltage but with reduced speed of the operation.

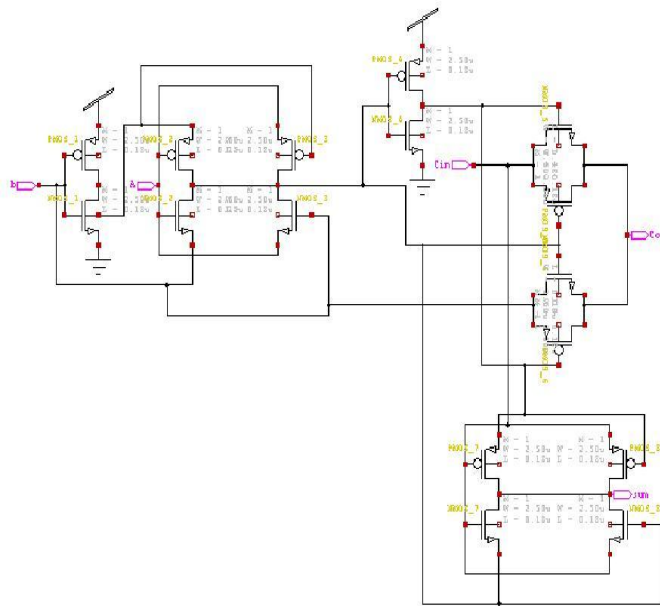


Fig.3 Schematic diagram of Existing full adder

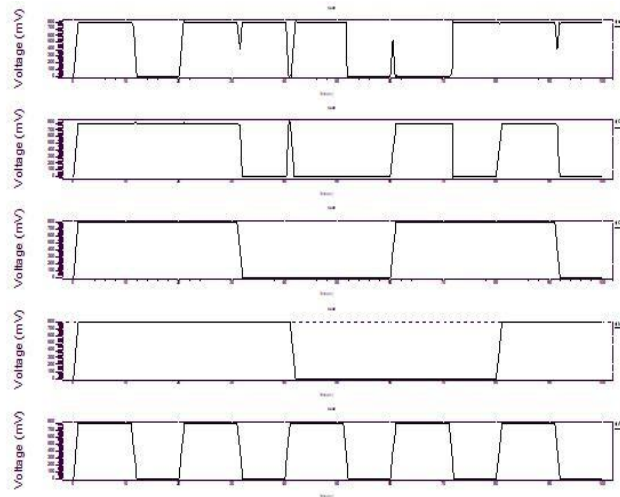


Fig.4 Input-Output waveforms of existing Full Adder

V. Proposed full adder circuit using MTCMOS technique

This paper focuses on the improvement of full adder for power and delay. Previously in existing circuit some leakage power dissipation problem; here we reduce this problem through MTCMOS technique [2]. In proposed circuit remove the disadvantage of the existing circuit. Here we make proposed circuit and compare to the existing circuit. The working of proposed full adder circuit can be explained using three blocks. Block 1 and Block 2 works as XNOR gate which generates the sum signal 'S' while Block 3 produces the output carry signal 'Cout'. Each block is designed separately to enhance power, delay and area. The proposed full adder circuit is shown in Fig.5.

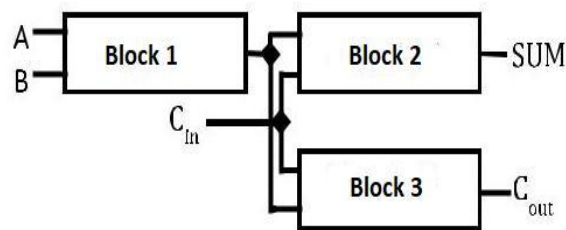


Fig.5 Diagram of Proposed Full Adder

The power consumption of full adder circuit depends on the X-NOR block. So this block is designed to reduce the power to a possible extent without any degradation in the voltage (V) of the circuit. Improved XNOR circuit is shown in Fig.5, here the power dissipation is reduced significantly using weak inverter designed by transistors pmos_1 and nmos_1. Pmos_3 and nmos_3 is used for full swing output. Transistors nmos_7 and nmos_8 are used for execution of carry output signal. The input carry signal C_{in} propagated by a single pass transistor nmos_7.

Pmos_6 and nmos_6 are connected to nMOS and pMOS transistor. MTCMOS is the low power techniques which reduce the leakage power dissipation in this circuit. We get better performance in terms of power, speed. Proposed full adder is designed by using MTCMOS technique, which is shown in Fig. 6 and Input-output waveforms of this circuit, is presented in Fig.7

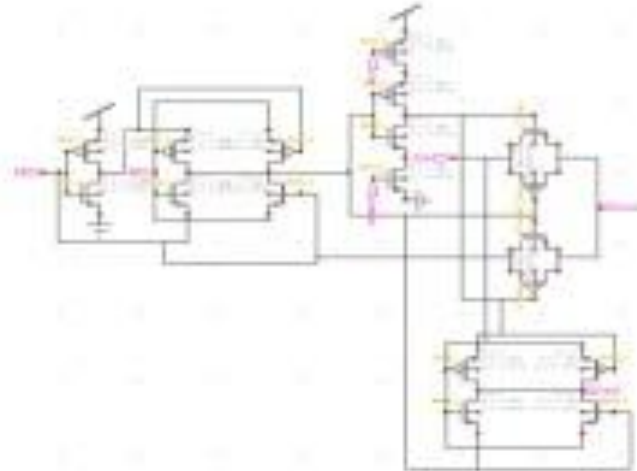


Fig.6 Proposed Full Adder Circuit by MTCMOS Technique

It reduces approx. 50% power consumption compared to the existing circuit, the performance of the circuit is better as compared to the existing circuit.

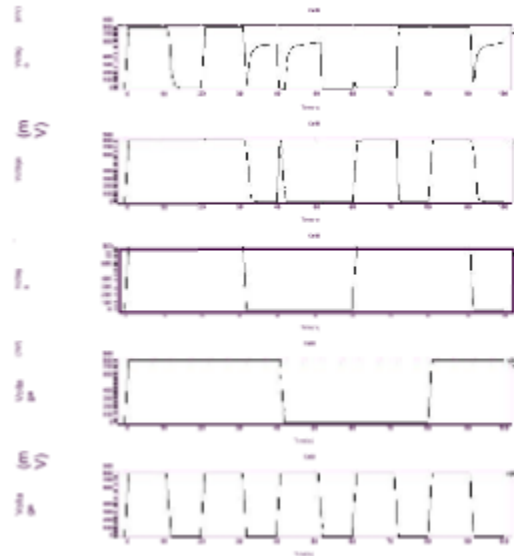


Fig.7 Waveform of Proposed Full Adder

VI. Simulation Result

The entire simulation of full Adder circuit has been done using Tanner EDA tool on 45nm technology. A detailed analysis of average power consumption and delay of adder on different technologies is presented here so that it can be used for high speed & low power applications, technology. It also decreases average power of the circuit up to certain extent. These results can be used for various low power and high speed applications. Comparison of various parameters of existing or proposed full adder is shown in Table I.

Parameters Circuits	Voltage (V)	Average time delay(sec)	Average Power consumption (watt)	No of Transist or
Existing Full Adder	0.6	5.15×10^{-11}	3.23×10^{-6}	16
Proposed Circuit		5.05×10^{-11}	2.078×10^{-6}	18
Existing Full Adder	0.8	5.105×10^{-10}	9.878840×10^{-6}	16
Proposed Circuit		5.001×10^{-10}	5.825796×10^{-6}	18
Existing Full Adder	1	4.85×10^{-9}	4.6×10^{-9}	16
Proposed Circuit		2.57×10^{-5}	1.32×10^{-5}	18
Existing Full Adder	1.4	6.123×10^{-8}	6.15×10^{-10}	16
Proposed Circuit		9.98×10^{-5}	4.48×10^{-5}	18
Existing Full Adder	2	2.023×10^{-7}	2.00×10^{-10}	16
Proposed Circuit		9.23×10^{-4}	3.90×10^{-4}	18

VII. Conclusion

Tanner EDA tool is used for the designing of all the circuits at 45nm technology, at a supply voltage of 2V, 1.4V, 1V, 0.8V and 0.6V are compared in table-I, and finally the best designs for the particular parameters are been concluded.

The existing full adder circuit has large power consumption and more delay. So to overcome this limitation a new circuit has been proposed. Power consumption of a circuit can be reduced using MTCMOS. So the proposed circuit is implemented using this technique. Although, the transistor count has increased, but the circuit has better power consumption and lower delay. MTCMOS adders occupy more area compared to the CMOS adders but the overall power dissipation is reduced.

In future this circuit can be used to design n-bit adder circuits (where $n = 2^k$; $k=0, 1, 2, \dots, k$). The designed full adder is found to have better performance than the adders available till now.

VIII. References

- [1] Bhattacharyya P, Kundu B, Ghosh S, Kumar V, Dandapat A. Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit. *IEEE Transactions on very large scale integration (VLSI) systems*. 2015
- [2] Nirmal, Uma, Geetanjali Sharma, and Yogesh Misra. "A low power high speed adders using MTCMOS Technique." *IJCEM International Journal of Computational Engineering & Management* 13 (2011).
- [3] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, "A novel low-power full-adder cell for low voltage," *VLSI J. Integr.*, vol. 42, no. 4, pp. 457–467, Sep. 2009.
- [4] C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, "A low-power high-speed hybrid CMOS full adder for embedded system," in *Proc. IEEE Conf. Design Diagnostics Electron. Circuits Syst.*, vol. 13, Apr. 2007, pp. 1–4.
- [5] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," *IEEProc.-Circuits Devices Syst.*, vol. 148, no. 1, pp. 19–24, Feb. 2001.
- [6] M. Zhang, J. Gu, and C.-H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in *Proc. Int. Symp. CircuitsSyst.*, May 2003, pp. 317–320.
- [7] Chowdhury, S.R., Banerjee, A., Roy, A., Saha, H., 2008. A high speed 8 transistor full adder design using novel 3 transistor XOR gates. *Int. J. Electron. Circ. Syst.*, 2(4): 217–223.
- [8] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.
- [9] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, "A novel low-power full-adder cell for low voltage," *VLSI J. Integr.*, vol. 42, no. 4, pp. 457–467, Sep. 2009.
- [10] A. M. Shams and M. Bayoumi, "A novel high- performance CMOS 1-bit full adder cell," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.* vol. 47, no. 5, May 2000, pp. 478–481.